CLAIMS

1. A manufacturing process for a silicon epitaxial wafer comprising the steps of:

forming an epitaxial layer on a silicon substrate with an interstitial oxygen concentration in a range of from 4 x $10^{17}/cm^3$ to 10 x $10^{17}/cm^3$ at a temperature of 1000°C or higher to obtain a silicon epitaxial wafer; and

applying heat treatment to the silicon epitaxial wafer at a temperature in a range of from 450°C to 750°C.

2. The manufacturing process for a silicon epitaxial wafer according to claim 1, wherein the interstitial oxygen concentration is in a range of from 6 x $10^{17}/cm^3$ to 10 x $10^{17}/cm^3$.

3. The manufacturing process for a silicon epitaxial wafer according to claim 1 or 2, wherein the heat treatment temperature is in a range of from 500°C to 700°C.

4. The manufacturing process for a silicon epitaxial wafer according to any of claims 1 to 3, wherein a substrate resistivity of the epitaxial wafer is 0.02 Ω-cm or lower.

5. The manufacturing process for a silicon epitaxial wafer according to any of claims 1 to 4, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.